REMARKS

By this amendment, claims 35, 37, 42-43, and 49-50 have been amended. New claim 51 has been added. Claims 35-37 and 40-51 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 37, 41, and 49 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims have been amended to address the concerns raised in the Office Action. Applicant respectfully requests that the rejection of these claims be withdrawn and the claims allowed.

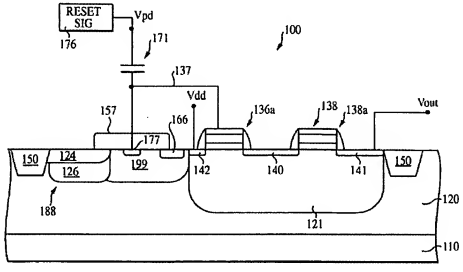
Claims 35-37, 40, 42-43, 45, and 49-50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhao (US 6,339,248) in view of Kochi (US 6,670,990). This rejection is respectfully traversed. In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. The Zhao and Kochi combination fails to teach or suggest all of the limitations of independent claims 35 or 42.

For example, claim 35 recites a pixel comprising "a reset region of a first conductivity type fabricated in said substrate and coupled to said charge collection region ... configured to apply a reset charge to said charge collection region in response to a pulsed reset signal applied to said reset region; a pulsed voltage source for providing said pulsed reset signal; and a capacitor, said capacitor having a first terminal in electrical communication with said pulsed voltage source and a second terminal in electrical communication with said reset region, wherein said charge collection region is reset solely through a signal supplied by said capacitor" (emphasis added). As described in the specification at paragraph [0005], the claimed invention

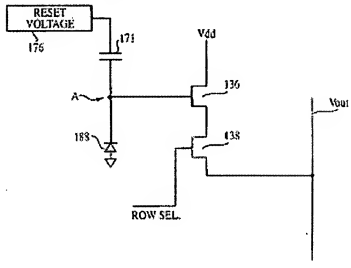
allows the conventional reset transistor to be omitted. *See* FIGs. 7 and 9, reproduced below. Applicant respectfully submits that Zhao and Kochi do not teach or suggest these limitations.

Claim 42 recites a pixel comprising "a charge collection region provided in a substrate; a reset region consisting of a doped region provided in said substrate, said reset region being adjacent said charge collection region for periodically resetting a charge level of said charge collection region ...; a source follower transistor ...; a pulsed voltage source ...; and a capacitor in electrical communication with said pulsed voltage source, said reset region, and said source follower transistor for storing charge collected in said charge collection region" (emphasis added). As described in the specification at paragraph [0005], the claimed invention allows the conventional reset transistor to be omitted. *See* FIGs. 7 and 9, reproduced below. Applicant respectfully submits that Zhao and Kochi do not teach or suggest these limitations.

Specification FIG. 7



Specification FIG. 9



To the contrary, Zhao teaches that a reset signal RESET is applied to a reset gate 121, which is not in the P substrate 101 of the Zhao active pixel sensor device. FIG. 8 (reproduced below). Applicant respectfully submits that Kochi does not disclose, teach, or suggest that the charge collection region is reset solely through a signal supplied by said capacitor as recited in claim 35. Nor does Kochi disclose, teach, or suggest that the reset region consists of a doped region provided in the substrate, as recited in claim 42. As described in the specification at paragraph [0005], the claimed invention allows the conventional reset transistor of Zhao to be omitted.

Zhao FIG. 8

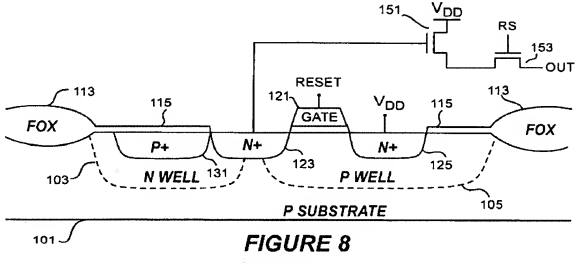
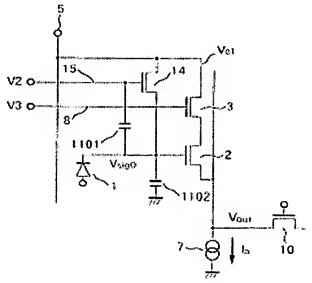


FIGURE 8

Nor does Kochi teach or suggest these limitations. Rather, Kochi teaches in FIG. 14 (reproduced below) that "1101 is a first capacitor formed between the gate of the reset switch 114 and the gate of the MOS transistor 102." Col. 15, ln. 51-53 (emphasis added). Furthermore, Kochi teaches that "the gate voltage of the MOS transistor 102 is reset to a voltage determined on the basis of potentials of the source, gate, drain, and well of the reset switch 114." Col. 15, ln. 58-61. Therefore, the entire reset transistor is required for Kochi to function.

Kochi FIG. 14



Kochi further teaches that "1102 denotes a second capacitor formed between the gate of the MOS transistor 102 and ground." Col. 15, ln. 55-57 (emphasis added). Therefore, Kochi's capacitor 1102 cannot read on the capacitor as recited in the claimed invention.

Applicant respectfully submits that Kochi does not disclose, teach, or suggest that the charge collection region is reset solely through a signal supplied by said capacitor as recited in claim 35. Nor does Kochi disclose, teach, or suggest that the reset region consists of a doped region provided in the substrate, as recited in claim 42. As

described in the specification at paragraph [0005], the claimed invention allows the conventional reset transistor 14, 104 of Kochi to be omitted. Therefore, Kochi does not remedy the deficiencies of Zhao.

Moreover, the Supreme Court recently said in *KSR Int'l Co. v. Teleflex Inc.* that "the [Graham] factors continue to define the inquiry that controls" a finding of obviousness and reiterated that a "patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." 127 S. Ct. 1727, 1734 (U.S. 2007). The Graham factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966).

Applicant submits that the Final Rejection has not properly shown that the Applicant's claims would have been obvious by conducting an examination of the Graham factors. "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. § 2141. Instead, to show that Zhao and Kochi may be properly combined and that the Applicant's claims are obvious in light of these references, the Final Rejection merely stated that it would be obvious to combine the capacitor of Kochi with the pixel of Zhao "to widen the dynamic range of the pixel and obtain image signals of a higher source/noise ratio." Final Rejection at p. 5. This statement is not an adequate substitution for an analysis of the Graham factors and does not show obviousness.

Since Zhao and Kochi do not teach or suggest all of the limitations of claims 35 and 42, claims 35 and 42 are not obvious over the cited combination. Claims 36-37, 40, 43, 45, and 49-50 depend, respectively, from claims 35 and 42, and are patentable at

least for the reasons mentioned above, and on their own merits. For example, claim 45 recites that the "reset region is doped with an n-type dopant at a first dopant concentration." Zhao, which has been cited for teaching this limitation, does not teach or suggest any dopant type for reset gate 121, which receives the reset signal RESET. *See* FIG. 8 above.

In addition, claims 49 and 50 recite that "said pulsed voltage source is operable such that said charge level of said charge collection region is reset both before and after charge is collected in said charge collection region" (emphasis added). The Final Rejection at page 7 cites to Kochi's FIG. 1 prior art circuit (Col. 2, ln. 18-20) for teaching resetting before the charge is collected. The Final Rejection then cites to completely different circuits with different operations: Kochi's FIG. 3 prior art circuit (Col. 3, ln. 42-45), and also to Kochi's alleged invention to teach resetting after charge is collected. Nowhere does the Final Rejection cite to, nor does Kochi teach or suggest, a single embodiment disclosing resetting both before and after charge is collected, as recited in claims 49 and 50.

Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 35-37, 40, 42-43, and 45 be withdrawn and the claims allowed.

Claims 41 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhao in view of Kochi, and further in view of Dasgupta (US 6,146,939). This rejection is respectfully traversed. Claims 41 and 44 depend from claim 42 and are patentable at least for the reasons mentioned above. Therefore, Dasgupta does not remedy the deficiencies of Zhao and Kochi.

In addition, claims 41 and 44 recite that the "charge capacitor has a charge-per-unit area capacitance value of about 5 $fF/\mu m^2$ to about 10 $fF/\mu m^2$." The specification

recites at paragraph [0038] that the capacitor should have a relatively high charge-per-unit capacitance. Dasgupta teaches a low charge-per-unit capacitance of 0.035 to 0.043 $fF/\mu m^2$. Col. 1, ln. 38-39. The minimum of the claimed range is more than 10000% of the maximum charge taught by Dasgupta. There is no overlap of ranges, and the only cited prior art has a range that is not even close to the claimed range. Although "obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties," the range taught by Dasgupta is not close at all, being less than 1/100 the minimum of the range. *Titanium Metals Corp. of America v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985). Therefore, Applicant respectfully submits that the gross difference in ranges shows unobviousness.

Moreover, Applicant submits that the Final Rejection has not properly shown that the Applicant's claims would have been obvious by conducting an examination of the Graham factors. Instead, to show that Dasgupta may be properly combined with Zhao and Kochi, and that the Applicant's claims are obvious in light of these references, the Final Rejection merely stated that it would be obvious to combine the references "since these values are in common use the similar capacitors in the art, as taught by Dasgupta." Final Rejection at p. 8. This statement is not an adequate substitution for an analysis of the Graham factors and does not show obviousness. Nor, does Dasgupta teach the claimed values, as discussed above. Furthermore, Dasgupta relates to general capacitors formed on substrates (Col. 1, ln. 9-10), and does not relate at all to the pixel circuits of Zhao and Kochi (or the claimed invention). Therefore, one skilled in the art would not look to Dasgupta to modify the inventions of Zhao or Kochi.

Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 41 and 44 be withdrawn.

Claims 46-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhao in view of Kochi, and further in view of Wada (US 6,677,676). This rejection is respectfully traversed. Claims 46-48 depend from claim 42 and are patentable at least for the reasons mentioned above. Therefore, Wada does not remedy the deficiencies of Zhao and Kochi.

Moreover, claim 47 recites that the "contact region is doped with an n-type dopant at a second dopant concentration." However, Wada teaches in FIG. 8 that the contact region 53 has a p+-type dopant, and is made where "n-type ions are not implanted or diffused." Col. 12, ln. 22-27. Therefore, Applicant respectfully submits that Wada does not teach that the "contact region is doped with an n-type dopant," as recited in claim 47. Claim 46 recites that the "capacitor is connected to said reset region through a contact region." Wada, however, does not disclose, teach, or suggest any capacitor or capacitor connection. Wada teaches only "establishing good electrical connection between the contact 59 and the body region 52" of the transistor of FIG. 8, and does not mention any connection between a capacitor and reset region as asserted by the Final Rejection at page 9.

Additionally, Applicant submits that the Final Rejection has not properly shown that the Applicant's claims would have been obvious by conducting an examination of the Graham factors. Instead, to show that Wada may be properly combined with Zhao and Kochi, and that the Applicant's claims are obvious in light of these references, the Final Rejection merely stated that it would be obvious to combine the references "to establish a good electrical connection between the capacitor and the reset region." Final Rejection at p. 9. This statement is not an adequate substitution for an analysis of the Graham factors and does not show obviousness.

Furthermore, Wada relates to general methods of manufacturing semiconductor wafers (Col. 1, ln. 11-12), and does not relate at all to the pixel circuits of Zhao and Kochi (or the claimed invention). Therefore, one skilled in the art would not look to Wada to modify the inventions of Zhao or Kochi. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 46-48 be withdrawn.

New claim 51 recites limitations similar to claims 35 and 42, and is patentable at least for the reasons mentioned above and on its own merits.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: September 14, 2007

Respectfully submitted,

By

Thomas J. D'Amico
Registration No.: 28,371
Rachael Lea Leventhal
Registration No.: 54,266
DICKSTEIN SHAPIRO LLP
1825 Eye Street NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant